Two different approaches of power-integrity analysis and correlation with on-chip measurement

MediaTek, Inc., Hsinchu City Taiwan
(1) Oscar Ou (2)Chee-Kong Ung (3)Mizar Chang (4)Sean Huang (5)Bihqui Tiang

ANSYS, Inc ., Taipei City Taiwan
(1)Pei-Shen Wei (2)Ying-Jiunn Lai (3)Chan-Chiuan Lee

Abstract

- Voltage noise had become a major obstacle in improving xPU processor's energy efficiency, it is dominated by the resonance between the chip/package/board and chip current behavior. Also referred to as first-droop noise, It is generally believed to be the dominant supply noise source in modern high performance and low power consumption system.
- We presents two different simulation approaches for power integrity analysis in this paper: The "Chip Aware" and "System Aware" Power Integrity Signoff flow.
- From the view of chip aware power integrity signoff flow, designer must ensure the impact of package and board PDN for chip level power integrity is within budget. On the other side, system aware power Integrity flow, SI/PI engineers have to simulate full chip PDN for various types of modulated chip power model(CPM). In these flow, data consistency across chip, package and board is key to achieve correlated result from both side.
- This presentation will describes the modeling methods of these two flows in detail and we will also present the correlation between the results.
- The simulation models of the target xPU power domain includes CPM, package and printed circuit board model. The CPM model was extracted by the chip power sign-off tool with real FSDB files. A rigorous 3D MoM solver was used for package extraction of equivalent RLCG circuit. The board PDN model in S-parameter was extracted by the MoM/FEM 2.5D electromagnetic hybrid solver. All part of the system (chip, package and board) have decoupling capacitors connected to them.
- Simulation results and final correlation to silicon measurements will also be presented.

Motivation: Find out the consistency between two different power design approaches

- Low power chipset may suffer functional failure during xPU sudden increase of switch activities.
- Dynamic voltage drop is the main suspect in xPU power failure. The supply noise was determined by the resonance between chip/package/board and chip current activity, also referred to as first-droop noise. It's generally believed to be dominant supply noise source in modern high performance system.
- Two different approaches for power integrity analysis were presented in this study, chip-aware and system-aware simulation flows.
- We conclude this study by presenting:
  - The consistency between two different power integrity signoff approaches.
  - The correlation between simulations and on-die sensor measurements.

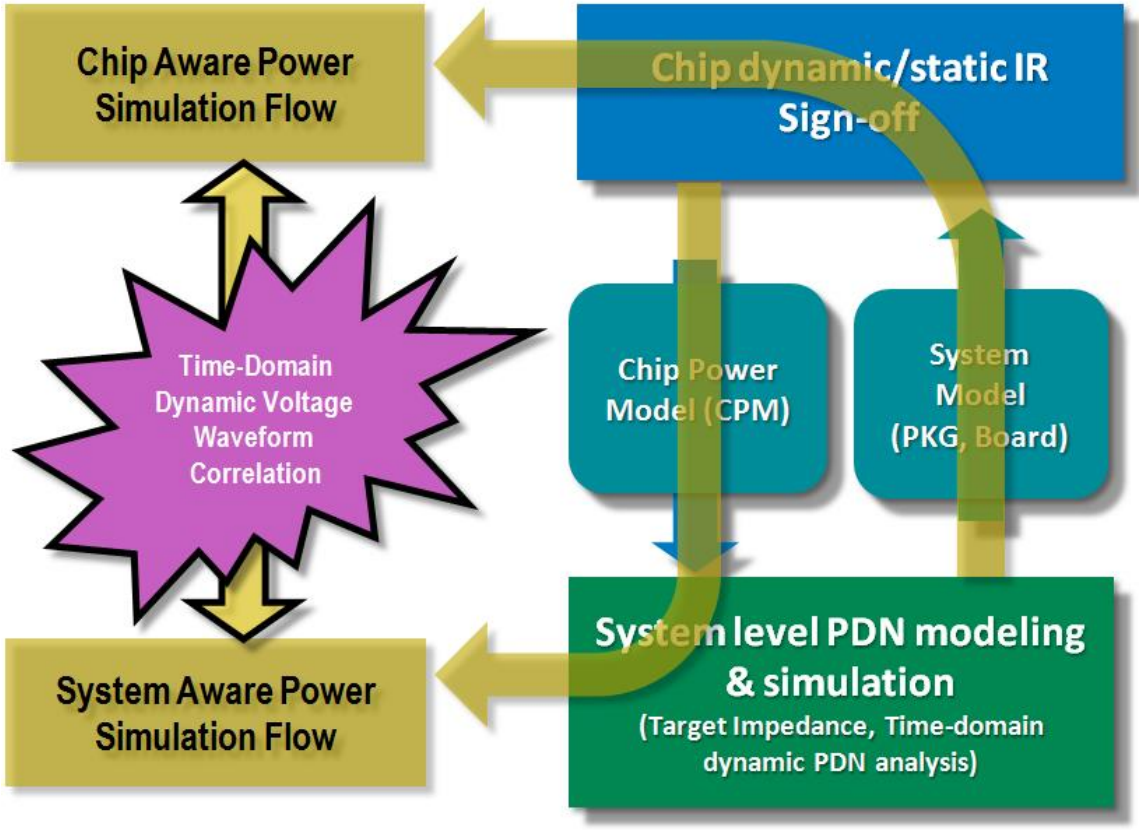


Fig.1. Above diagram shows two different approaches of Chip Package-System Co-analysis Flows

Main Idea-1: Power delivery network design

Power Delivery Network (PDN) in our case :

- Gated power network for xPU block was shown in Figure.2. With programmable gate control, the power gate can turn on/off to reduce xPU power consumptions. In this study the package routing was used for gated power network. Near bump on-die sensors were used for real-time voltage drop measurement.

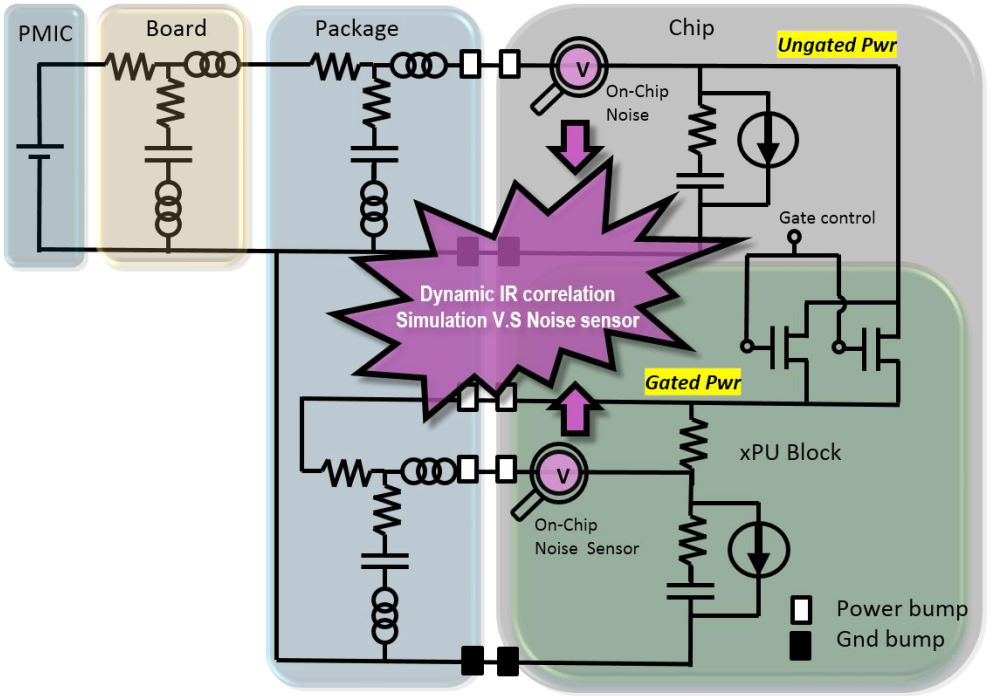


Fig.2. The schematic of gated power network with pre-designed chip noise sensor.

Main Idea-2 : PDN modeling from chip to board
- chip power model(CPM) with real functional pattern

1. **Use gate-level, true-time FSDB pattern.**
2. **CPM models were used to model chip in system level power integrity analysis, CPMs were composed of:**
   - **Header: chip package protocol (CPP) include pad location information for the connection between chip and Package.**
   - **Parasitic: spice compatible lump RLGC model with total >100 nodes that includes on-chip un-gated and gated power network.**
   - **Current model: Per-bumps current waveform with global ground node based on cell level timing and dynamic current consumption.**

CPM Extraction Flow

1. Setup Design → 2. Power Calculation → 3. PG Extraction → 4. CPM Creation

Inputs (example):

a. Tech → tech. file.
b. Def → Cell placement + power grid.
c. Lef → Macros used in design.
d. Lib → for power calculation.
e. FSDB → pattern.
f. etc.

Outputs:

a. Current profile for every domain.
b. Silicon Power Delivery Network (PDN).

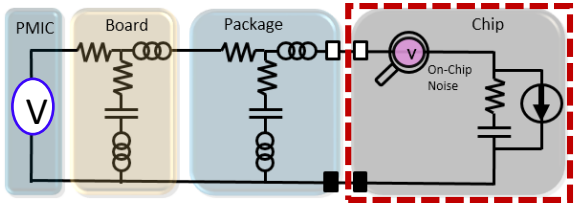
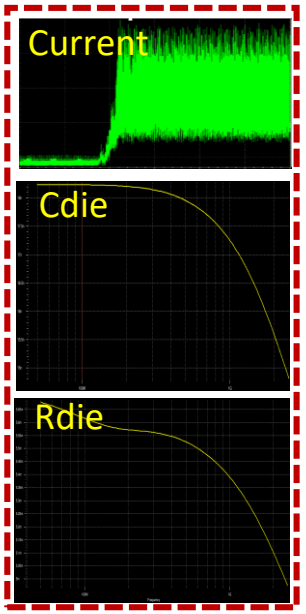


Fig.3. Illustration of Full PDN Connections

1. **Gate-level, true-time FSDB file.**
2. **RCdie with spice compatible RLGC model.**
3. **Current waveforms based on cell level timings and dynamic current consumption.**



4.a

4.b

Fig.4. Illustration CPM Extraction Outputs.

Package / Board Modeling

- **Package modeling:**
  - Per-bump resolution SPICE model includes nodes of decoupling capacitors. Parasitic are associated with every bump.
  - CPM contains the IC die power model and pin location (ploc). PLOC information enables PKG extraction tool to automatically align and connect the IC die pins and the package pins.
  - PKG model was extracted by ANSYS SIwave-CPA Q3D solver. It also supports 3D FEM-based solver extraction of power nets on package. (The theory of operation of different solver will be presented on next page)
- **PCB modeling:**
  - Using hybrid solver to extract board level power delivery network and export S-parameter which includes DC information and on-board de-coupling capacitors.

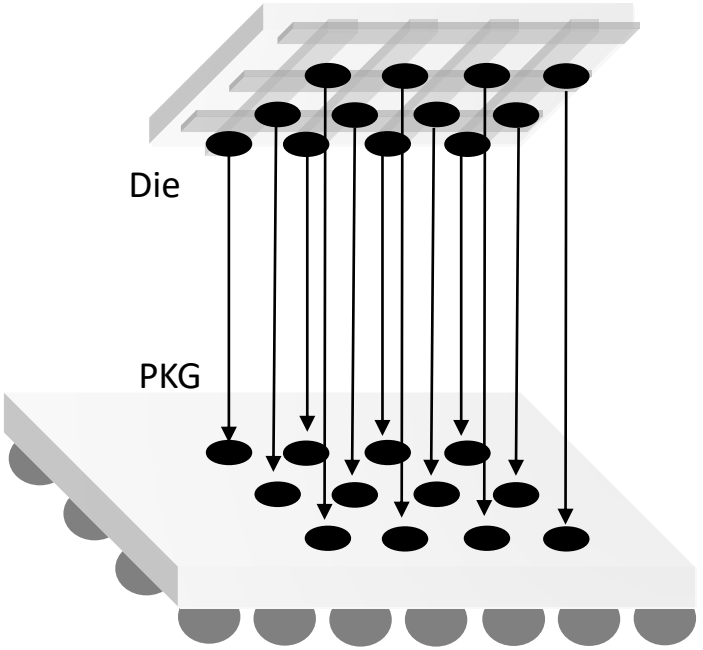


Fig.5. Pin location(ploc) information

Solver explanation/concept of Package modeling tool

- Maxwell's equations govern all electric, magnetic and electromagnetic (EM) behavior and play a particularly important role in the design of IC chips, packages and PCBs. A variety of numerical methods are available to solve the Maxwell's equations and two such popular methods are the Finite Element Method (FEM) and Method of Moments (MoM). Each of these techniques have unique advantages and their 3D versions are employed in ANSYS CPA.
  - **MoM:** MoM is an integral equation method and CPA-Q3D uses a 3D quasi-static formulation to solve for RL and CG. The solver is accelerated by the Fast Multipole Method (FMM). Results include proximity and skin effect, dielectric and ohmic loss, and frequency dependencies. The surfaces of conductors are discretized into a set of triangular patches, and an unknown charge is associated with each patch. By Coulomb's law, the potential $\phi(\vec{x})$ at a point $\vec{x}$ due to a distribution of charges $\rho(\vec{x})$ is given by the integral. Here S denotes the surfaces of all the conductors, and $\|\vec{x} - \vec{x}'\|$ is the Euclidean distance between points $\vec{x}$ and $\vec{x}'$. When such an integral equation is discretized into a finite set of surface patches, it leads to a large dense system of linear equations for CG computation.

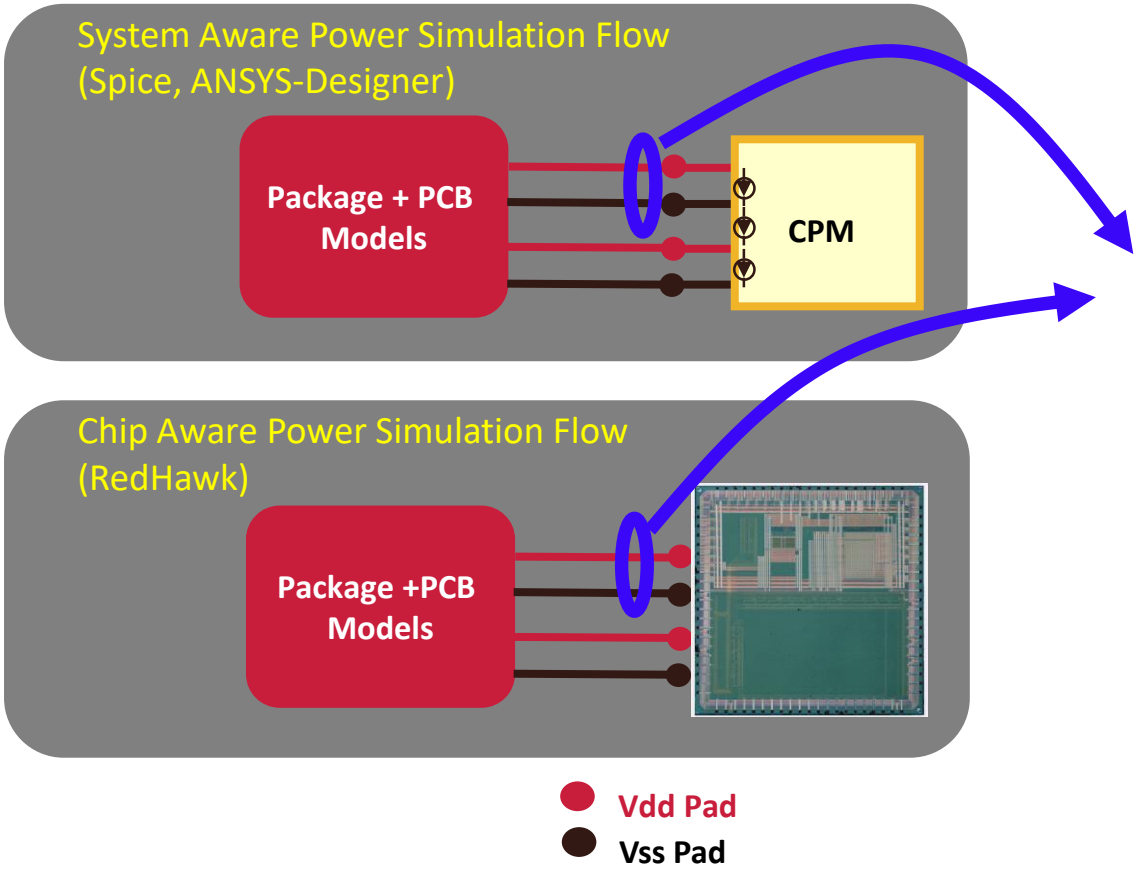
$$\phi(\vec{x}) = \int_S \frac{\rho(\vec{x}')}{4\pi\epsilon\|\vec{x} - \vec{x}'\|} dS$$

  - **FEM:** In contrast to the MoM approach described above which results in a dense system matrix, the FEM formulation gives rise to sparse matrix. EM solve the functional using a 3D volume mesh for all functions v(x). One of the advantages of FEM is that once the matrix is directly factorized, the cost of solving the system matrix equation for any number of excitation vectors is trivial. This allows the FEM solver in CPA to extract highly complex models with 1000's of bumps and large number of nets very efficiently.

$$\varphi(u, v) = \iint_D f(x)v(x)dD$$

- In this study, MoM solver was used for package modeling. As the problem size gets larger, the solution of dense MoM matrix could become computationally intensive even using iterative techniques. But smaller structures such as lead-frame packages, wire-bond structures, a small part of flip-chip package, etc. can be more efficiently handled by the integral-equation based MoM solver using adaptive meshing. For electrically larger structures such as large flip-chip packages, and those with large number of ports to be extracted, FEM solver gives a much better efficiency due to the afore-mentioned reasons

Voltage waveform comparison between two system and chip aware power simulation flows



Probing point is close to pre-designed on-chip noise sensor

Fig.6. Illustration of probe point

PDN diagram & probe point

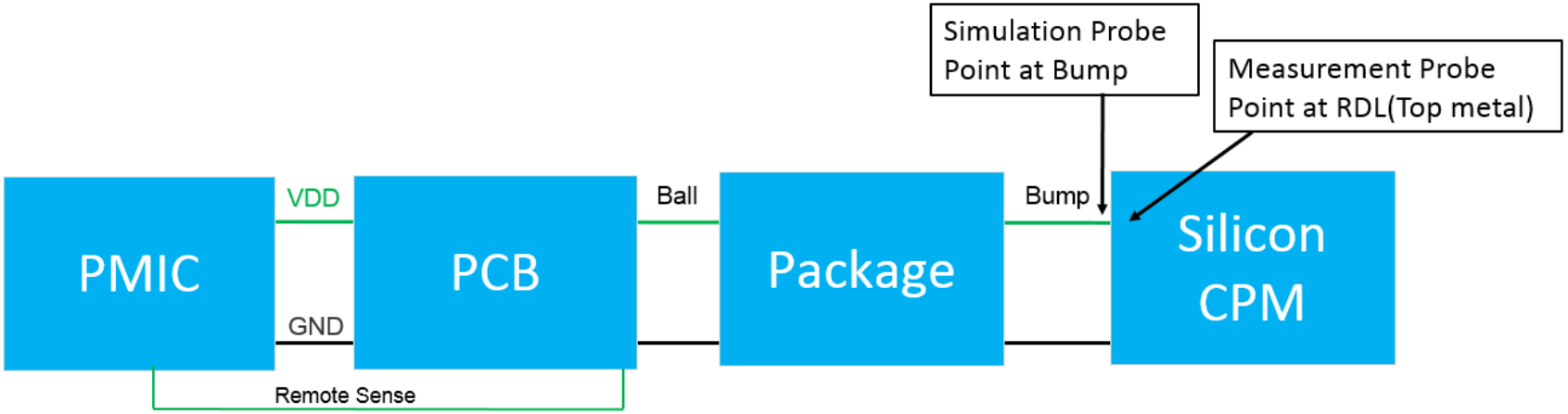


Fig.7. Illustration of PDN diagram

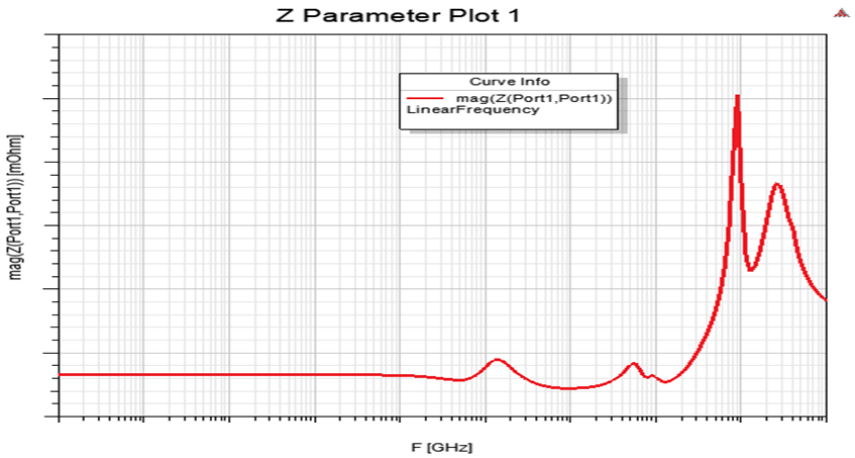


Fig.8. Illustration of PDN impedance profile

Evidence

- The simulation result between two power simulation flows correlated well.

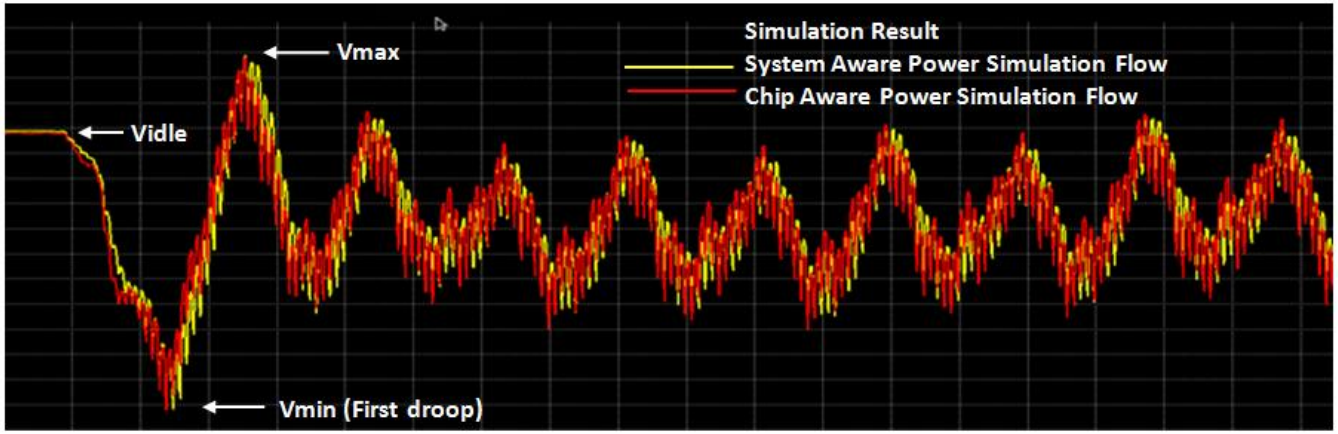


Fig.9. The simulation results of the two flows

- The correlation between simulation and on-die noise sensor measurement.
  - On-die noise sensor used comparator circuitry to detect voltage droop by comparing programmable Vref and VDD.

Main Idea	Normalized Delta to Msmt
1	0.95%
2	1.05%

Summary

- This study demonstrates two different simulation approaches for power integrity analysis in chip and system design. The results show that with correctly tuned flow, approaches from chip and system side can correlate well to each other.
- This study also shows voltage correlation between simulation and on-die sensor measurement to within 1.05% normalized difference.
- Future works: simulation time and accuracy improvements.
  - Higher pattern coverage slowed down CPM and on-chip IR simulation time.
  - Higher number of CPM ports slowed down transient simulation time drastically.
  - Measurement with transient waveform at bump instead of measurement with discrete value(Vmin) through Comparator to improve accuracy.